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Nanoslits in silicon chips

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Abstract

Potassium hydroxide (KOH) etching of a patterned ⟨100⟩ oriented silicon wafer produces V-shaped etch pits. We demonstrate that the remaining thickness of silicon at the tip of the etch pit can be reduced to ∼5 μm using an appropriately sized etch mask and optical feedback. Starting from such an etched chip, we have developed two different routes for fabricating 100 nm scale slits that penetrate through the macroscopic silicon chip (the slits are ∼850 μm wide at one face of the chip and gradually narrow to ∼100–200 nm wide at the opposite face of the chip). In the first process, the etched chips are sonicated to break the thin silicon at the tip of the etch pit and then further KOH etched to form a narrow slit. In the second process, focused ion beam milling is used to etch through the thin silicon at the tip of the etch pit. The first method has the advantage that it uses only low-resolution technology while the second method offers more control over the length and width of the slit. Our slits can be used for preparing mechanically stable, transmission electron microscopy samples compatible with electrical transport measurements or as nanostencils for depositing nanowires seamlessly connected to their contact pads.

S Supplementary data are available from stacks.iop.org/Nano/20/045303

1. Introduction

KOH etching of a ⟨100⟩ silicon wafer is anisotropic. KOH etches the ⟨100⟩ and ⟨110⟩ planes of single crystal silicon at a much higher rate than the ⟨111⟩ plane. This creates a V-shaped etch pit bound by the ⟨111⟩ crystal planes of silicon. This etching property of silicon is commonly used for making silicon nitride membranes. Large, ∼100 μm wide slits can be easily fabricated in bulk silicon wafers using standard photolithography and KOH wet etching [1]. Small, ∼100 nm wide slits can be fabricated in silicon-on-insulator (SOI) substrates [2, 3]. However, this method of nanoscale slit making cannot be directly extended to a bulk silicon wafer because it relies on the tiny thickness variation of the thin silicon layer in the SOI substrate [4]. Careful control of the KOH etching of bulk silicon wafers has allowed features in the sub-micrometre range such as silicon nanopores [5] and thin silicon membranes [6]. We demonstrate sub-micrometre slits fabricated in bulk silicon wafers using KOH etching, both with and without the assistance of focused ion beam (FIB) milling.

We observed that by carefully controlling the KOH etch of a silicon chip, the tip of the V-shaped etch pit can be brought to within ∼5 μm of penetrating the silicon chip. To do this, we periodically inspect the etch pit in an optical microscope with a strong back light. When the silicon is thin enough, visible light can penetrate through the thin silicon at the tip of the etch pit. Starting from a silicon chip with such an etch pit, we have developed two different processes of fabricating 100 nm scale slits that penetrate the silicon chip. In the first process, sonication breaks the thin silicon at the tip of the etch pit. Continuing the KOH from this point creates a narrow silicon nitride membrane (∼100–200 nm wide). Removing the silicon nitride membrane with a phosphoric acid strip creates a slit. We have produced slits down to 125 nm wide using this method. This process does not use FIB milling and the slits propagate the entire length of the etch pit. The second process uses FIB milling to etch through the thin silicon and silicon nitride at the tip of the etch pit. The first method uses only low-resolution technology while the second method offers greater control over the length and width of the slit (see figure 1). These slits are useful as substrates for combining electrical transport measurements and transmission electron microscope (TEM) imaging. We show TEM imaging with simultaneous *in situ* measurement of a multi-walled carbon nanotube (MWNT) deposited on a sonication-induced slit. We demonstrate TEM imaging and measurement of superconducting nanowires deposited on a FIB milled slit. The fragile superconducting nanowires would

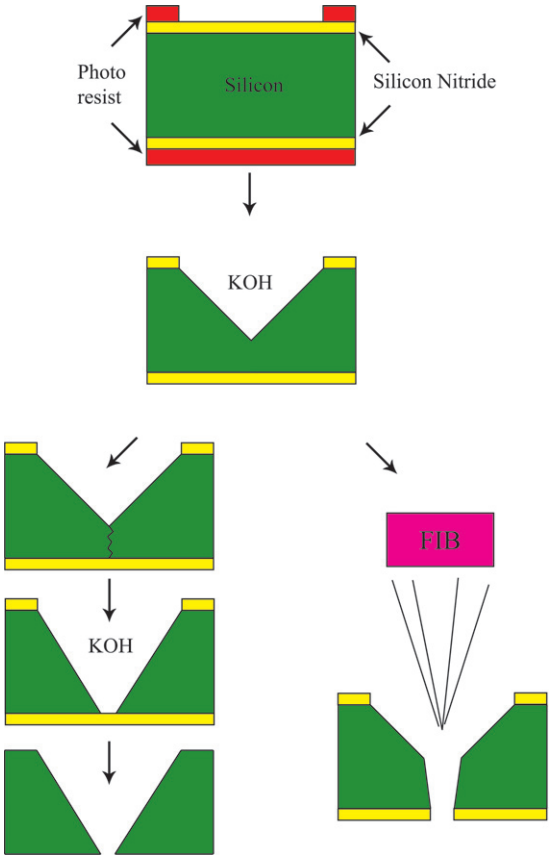

Figure 1. Two processes for fabricating nanoslits in macroscopic silicon chips: starting with a silicon wafer coated with silicon nitride, photolithography followed by reactive ion etching (RIE) is used to define a hard mask in the silicon nitride. KOH etching is used to produce a V-shaped etch pit. The KOH etch is monitored using optical microscopy. When the remaining silicon at the bottom of the etch pit is thin enough, light will penetrate through when the sample is back lit. From this point, two different fabrication routes can be followed. On the left, ∼100 nm scale slits are produced using only low-resolution technology. The thin silicon is first cracked using brief sonication in deionized water. Further KOH etching of the crack produces a silicon nitride membrane ∼100–200 nm wide. Stripping the silicon nitride produces a narrow slit. On the right, focused ion beam (FIB) milling is used to directly make ∼100 nm scale slits through the thin silicon. This method offers more control over the length and width of the slit than the process on the left but relies on high-resolution technology.

(This figure is in colour only in the electronic version)

typically not survive on a less mechanically stable TEM sample (such as slits in a silicon nitride membrane) because stress from handling of the sample or cryogenic cooling would fracture the nanowire.

The slits are also useful for nanostencil lithography. A nanostencil is nanoscale shadow mask typically consisting of a silicon nitride membrane with nanoholes or nanoslits micromachined into it. Nanowires or nanoparticles can be formed when material is deposited through the nanoholes or nanoslits in the nanostencil. A variety of nanoparticles and nanowires have been formed using this method [7–11]. We show a 200 nm wide gold nanowire fabricated by nanostencil deposition through a sonication-induced slit. The flexibility of a traditional silicon nitride membrane makes it difficult to fabricate certain patterns in a nanostencil. For instance, a nanostencil for one step deposition of a nanowire seamlessly connected to larger contact pads would require a thin slit connected to two larger holes. While this geometry would be unstable in a silicon nitride membrane nanostencil, our slits are supported by macroscopic silicon walls. We demonstrate deposition of a 330 nm wide gold nanowire seamlessly connected to its contacts using a FIB milled slit.

2. Experimental details

The silicon wafers used for this paper are 3″ diameter, ⟨100⟩ lightly n-doped Czochralski (Cz) double side polished (DSP) silicon wafers with 100 nm of low stress, low pressure chemical vapour deposition (LPCVD) silicon nitride deposited on both sides (Surface Process Group). The wafers are 600 ± 5 μm thick. A tight specification on thickness makes choosing the initial mask size easier. The wafers have a total thickness variation (TTV) <3 μm. A small TTV makes the point at which to stop the KOH etch fairly uniform across the wafer. Cleavage lines for the chips are defined by the KOH etch using a corner compensation technique to get rectangular chips [12]. Alternatively, rectangular chips can be defined by dicing after the KOH etch. A transparency mask (5080 dpi transparency printer) was used to define etch pits and cleavage lines using photolithography. We achieved the best accuracy in transparency masks by coding the mask directly in the postscript programming language accepted by the printer rather than using a computer assisted drawing program (CAD) and translating it to postscript. After photolithographic patterning with an appropriately sized mask, the pattern defined in the photoresist was transferred into the silicon nitride by reactive ion etching (RIE) using a CHF_3/O_2 plasma. The photoresist was then stripped in acetone.

The wafer was placed in 70 °C KOH (45% by weight Sigma Aldrich) to etch the silicon anisotropically. A timed etch was performed using a programmable hotplate (Torrey Pines Scientific HS40). Empirically, we found a time of 6 h to be a satisfactory starting point. At the end of 6 h, the hot plate automatically switches off. The actual initial etch is longer than 6 h since etching continues as the KOH etchant cools. Because the ⟨111⟩ plane etches much more slowly than the ⟨100⟩ or ⟨110⟩ plane, a V-shaped etch pit is produced. After the initial etch, etching is continued as before but is now monitored at periodic intervals. Every 15–30 min, the wafer is removed from the KOH and placed in a flat polystyrene petri dish (FALCON 351007) filled with the minimum amount of deionized water needed to cover the sample. The wafers are inspected in an optical microscope with a strong back light (VWR VistaVision T-RTP). When the silicon is sufficiently thin (we estimate ∼5 μm from FIB cross sections), a thin red line will be visible in the optical microscope from the back light penetrating the chip. At this point, KOH etching is stopped by a rinse in deionized water, nitric acid, deionized water, and then isopropanol. The wafer is then blown dry with nitrogen gas. These ‘red-line’ samples are the starting point for the various processes described. Using a wafer with a

tight TTV as described, the majority of the wafer will become 'red-line' chips at around the same time. The chips were cleaved and separated at this point before further processing was performed to minimize stress on the slit. The mask used was designed by calculating the width of the mask required to just etch through the wafer. Using simple trigonometry, it can be derived (from the angle the etch pit makes relative to the surface of the chip, $\tan^{-1}\sqrt{2} \cong 54.7°$) that this width follows the formula $w = h\sqrt{2}$ where h is the thickness of the wafer and w is the width of the mask required to just etch through the wafer. For a 600 μm thick wafer, the width of the mask should be $600 \times \sqrt{2} \cong 849$ μm. The variation in wafer thickness of ± 5 μm implies the mask width should be between $595 \times \sqrt{2} \cong 841$ μm and $605 \times \sqrt{2} \cong 855$ μm. Because we manually align to the flat of the wafer, we get some undercut from the etch so an undersized mask was used. If we use only one size mask, the etching time can vary by several hours just from the variation in thickness between separate wafers. Therefore, we performed a test etch with varying size etch pits on a small piece of the wafer. The test mask had etch pits ranging from 790 to 830 μm in 5 μm increments. The test mask and corresponding wafer sized masks can all be included on a single transparency.

We have also tried this fabrication process on wafers with a much larger uncertainty in thickness (± 25 μm). The large variation in thickness made it more difficult to choose an appropriate sized photomask. We had to use a significantly under sized mask and use long etching times. If the photomask used is significantly undersized, the KOH etch cannot be completed in a reasonable amount of time (several hours). In this case, tetramethylammonium hydroxide (TMAH) (Sigma Aldrich) etch was used since it etches the ⟨111⟩ plane of silicon more quickly than KOH. In this case, we did an etch of TMAH for 3 h and KOH etch for 1 h until we reached a red-line state. However, with more uniform wafers, a properly sized mask and a test mask, this step was unnecessary. Wafers with less tight TTV's tended to reach the red-line state at different etching times across the wafer. This required stopping the etch when some of the samples were ready, separating out samples that were not ready and continuing the etch independently for each samples that did not yet have light penetrating it when back lit. Using a wafer with TTV <3 μm had most of the wafer reach the red-line state at roughly the same time and allowed stopping of the etch on the entire wafer simultaneously.

Once a 'red-line' chip is formed, we can fabricate ∼100 nm scale slits in it using only sonication and wet etching. A 'red-line' chip is briefly (less than 1 s) sonicated in deionized water. This sonication breaks the silicon along the thinnest point, which is the tip of the V-shaped etch pit. The silicon nitride on top of the silicon does not typically break. The chip is then etched in 70 °C KOH for 1–5 min. Every 30 s, the chip is removed from the KOH, placed in a petri dish with the minimum amount of DI water needed to cover the chip and examined under an optical microscope. When the slit appears to have etched to an appropriate size, the chip is cleaned in nitric acid, deionized water, isopropanol and then blown dry with nitrogen gas. Once dry, the chip is inspected under the optical microscope again. Although the optical microscope is inherently inaccurate at this small scale, we have produced slits down to 125 nm wide (see figure 2). The inaccuracy of the optical microscopy feedback and sizing by eye produces a spread in slit sizes of ∼100 nm amongst different chips. A more accurate form of feedback than the optical microscope should allow smaller slits and a smaller spread in slit size. The silicon nitride typically survives to form a membrane across the narrow silicon slit. To form an actual slit, the silicon nitride is stripped in 115 °C phosphoric acid for 40 min. A few isolated sections of the slit are unusable from damage done by the sonication step but the majority of the slit is a usable, uniform ∼100–200 nm slit. Variation in the slit width appears to depend mostly on the sonication step and not surface roughness of the KOH etch (we did not measure surface roughness of the KOH etch). The use of 45% KOH at 70 °C and the short duration of the final KOH etching step should minimize the effects of surface roughness from the KOH etch. Without the sonication step, the Cz silicon does not open up into a uniform slit. We have also tried this fabrication process with float zone (Fz) silicon wafers with LPCVD silicon nitride on both sides (SVMI). Fz wafers can be opened up into a slit on the order of 100 nm wide without the sonication step described for Cz silicon. This is because Fz crystal is intrinsically more pure than Cz crystal because of oxygen absorbed during formation of Cz silicon. However, Fz crystal is also intrinsically more fragile than Cz crystal. Thus slits formed in Fz silicon often had cracks running parallel to the slit, making them unusable (see supplementary data available at stacks.iop.org/Nano/20/045303). Slits formed in Cz silicon rarely display cracks. However, Cz samples do not open into a 100 nm scale slits from KOH etching alone but typically form a triangular shape slit propagating from one end of the

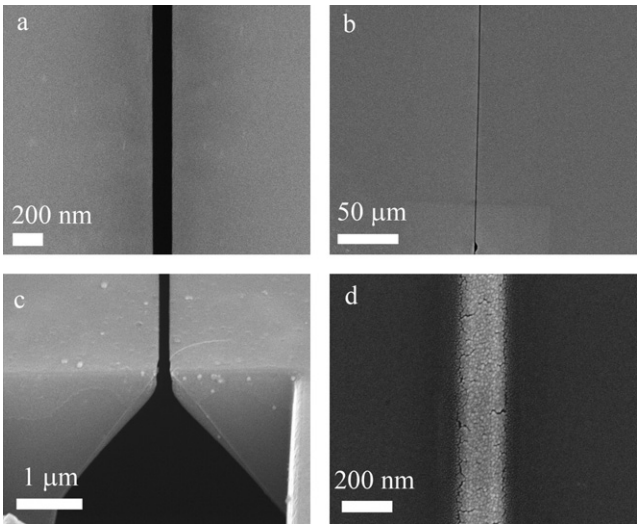

Figure 2. (a) Close-up of 125 nm slit formed using only transparency mask photolithography, sonication and wet etching (b) the slit shown in (a) remains 125 nm for over 100 μm. A small, isolated damaged region can be seen at the bottom of the micrograph (c) a cross section milled by the FIB of a slit formed by photolithography, sonication and wet etching. (d) A 200 nm nanowire formed by nanostencil deposition through a slit formed using only photolithography, sonication and wet etching.

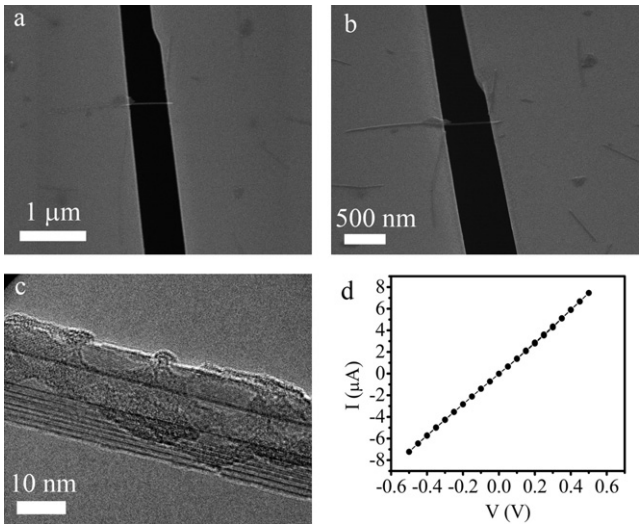

Figure 3. (a) A scanning electron microscope (SEM) micrograph of a multi-walled carbon nanotube (MWNT) suspended across a TEM compatible slit made only with transparency mask photolithography, sonication and wet etching. The sample was oxidized and gold electrodes were deposited before the nanotube was deposited, so a transport measurement could be made. (b) An SEM micrograph of the same MWNT shown in (a) taken at 52° tilt. (c) A TEM micrograph of the same MWNT shown in (a) and (b). (d) Current versus voltage graph for the same nanotube shown in (a), (b) and (c) measured *in situ* in the TEM. The particular nanotube measured appears to be metallic with a two-probe resistance of 69 kΩ. This high resistance is most likely contact resistance due to the short length of the contact between the gold electrode and the nanotube as can be seen on the right-hand side in the SEM images (a) and (b). This is a demonstration graph showing these slits can be used for TEM imaging and *in situ* measurement simultaneously. The error bars are smaller than the points on the graph.

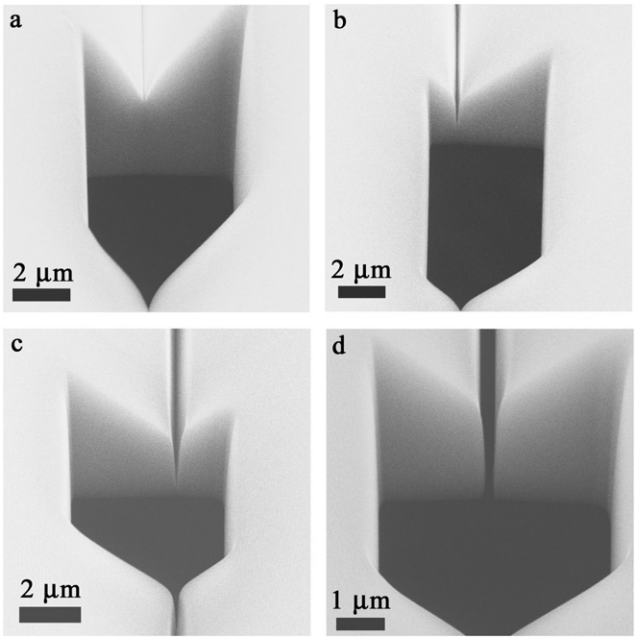

Figure 4. (a) SEM image of an FIB milled cross section of the etch pit side of an unmodified 'red-line' chip viewed at 52° tilt (b) after 30 s of etching a 30 μm long slit with an FIB beam of 3000 pA from the etch pit side viewed at 30° tilt (c) after 45 s of etching a 30 μm long slit with an FIB beam of 3000 pA from the etch pit side viewed at 30° tilt (d) after 60 s of etching a 30 μm long slit with an FIB beam 3000 pA from the etch pit side viewed at 30° tilt. The slit penetrates the silicon and is 200 nm wide. The slits and cross sections shown in (a)–(d) were etched on different portions of the same sample. The slit was cut before the cross section was cut.

etch pit. This triangular shape was avoided by introducing the sonication step described.

These sonication-induced slits can be used as nanostencils. We inverted a 125 nm slit onto a silicon nitride membrane and deposited 5 nm of titanium and 30 nm of gold using e-beam evaporation. This resulted in a 200 nm wide nanowire (see figure 2). The nanowire's larger width compared to the slit indicates that conformal contact between the slit and the substrate were not made. The conditions for nanostencil deposition were not optimized.

We also use these sonication-induced slits to perform simultaneous TEM imaging and *in situ* electrical transport measurement on individual multi-walled carbon nanotubes (MWNT's). After the silicon nitride is stripped from the silicon chip, thermal oxide is grown on the silicon for electrical insulation. The slit was shadow masked with strips of polydimethylsiloxane (PDMS, Sylgard 184). To form electrodes, 5 nm of Ti and 30 nm of gold were evaporated onto the slit at 5×10^{-6} Torr. Slits for transport measurements were purposefully made larger than 100 nm because the thermal oxide growth and subsequent deposition of metal reduce the width of the final slit. MWNT's were applied by crushing MWNT powder between two pieces of PDMS and then applying the PDMS to the slit [13, 14]. Unwanted nanotubes and debris crossing the slit were removed using FIB milling. Care was taken so the nanotube to be measured was not exposed to the ion beam. The sample was mounted in a specially designed TEM specimen holder that allows electrical contact to the sample *in situ* [15]. Electrical transport measurements and simultaneous TEM imaging were performed (see figure 3). The particular MWNT measured in figure 3 appears to be metallic with a two-probe resistance of 69 kΩ. This relatively high resistance is most likely contact resistance due to the short length of the contact between the gold electrode and the nanotube [16] (see the right-hand side of the slit in figures 3(a) and (b)).

For the most mechanically stable TEM compatible samples that can also be used for transport measurements, slits are cut in the 'red-line' chips using a FIB. FIB milling takes place from the etch pit side. Because the thickness control of the thinnest point is only feedback by eye from an optical microscope, the time needed to cut through the silicon must be varied. Initial ion currents used are 1000–3000 pA. Milling times were 1–10 min for a 40 μm long slit. We determined the appropriate etching time by cutting a cross section that showed whether a given FIB cut penetrated or not. When an FIB cut is close to being through, the ion current can be reduced to 100–300 pA for the final cut. Alternatively, an ion detector beneath the sample would allow *in situ* determination of the breakthrough point. Slits down to ∼150–200 nm wide can routinely be fabricated. The slits formed are very stable by nature of their construction (see figure 4).

We formed superconducting nanowires across FIB milled slits using molecular templating [17]. Carbon nanotubes are deposited across the slit and superconducting metal is deposited on them by a DC sputtering process. FIB milling is used to remove extra nanowires and separate the two electrodes defined by the slit. Alternatively, photolithography followed by wet etching can be used to remove the extra nanowires and define the electrodes. Care is taken so the nanowire to be measured is not exposed to the ion beam. The resistance versus temperature curve of the nanowire formed on this type of slit shows the same behaviour as superconducting nanowires formed on more conventional non-TEM compatible trenches (see figure 5) [17–19]. Resistance versus temperature measurements on superconducting nanowires fabricated on less stable TEM compatible slits did not show the same behaviour or even go superconducting, typically because of cracks in the nanowire. Sonication-induced slits were not sufficiently mechanically stable for superconducting nanowires because the slit propagates the entire length of the etch pit (1 mm). FIB milled slits are much more mechanically stable because the slit can be made shorter than the length of the etch pit and the supporting silicon near the edge of the slit is significantly thicker (∼5 μm thick for FIB milled slits compared to a few 100 nm for the sonication-induced slits). We observed that superconducting nanowires formed on slits 100 μm or longer routinely showed cracks in the nanowire (see supplementary data available at stacks.iop.org/Nano/20/045303). Nanowires on slits 40 μm long or shorter showed similar behaviour to nanowires fabricated on more conventional non-TEM compatible samples. Cooling the sample slowly (by not including exchange gas) helped ensure the nanowire survived the resistance versus temperature measurement. We had difficulty routinely depositing SWNT's that lay fully on top the slits by solution deposition. SWNT's that did not lie fully on top of the slit showed signs of bad contacts (visible by SEM imaging) between the wire and the contact pad after metal was deposited on them. Using the PDMS deposition method described, we can routinely deposit MWNT's but not SWNT's that are fully on top of the slits. Superconducting nanowires fabricated on MWNT's on our TEM slits showed the same behaviour as superconducting nanowires fabricated on MWNT's on regular non-TEM compatible trenches. Superconducting nanowires fabricated on MWNT's typically have multiple transitions as they go superconducting, unlike the superconducting nanowires fabricated on SWNT's, because MWNT's have a larger diameter than SWNT's thus affecting the geometry of the nanowire.

For use as nanostencils for nanowires with seamless connected contact pads, FIB milling in a different pattern was used. A 'red-line' chip was fabricated as described above. At the tip of the V-shaped etch pit, a few 10 μm by 10 μm holes piercing the silicon were cut from the etch pit side. The chip was then flipped over and FIB etching proceeded from the front. The holes cut from the etch pit side aided in locating the thin silicon at the tip of the V-shaped etch pit when imaging from the front side. An area was selected above the etch pit and scanned with an ion beam of 5000 pA. The area scanned gradually etches down until the thinnest section breaks through. Breakthrough occurred at the edge of the area scanned. At this point, the ion current was reduced to 500 pA and scanning proceeded until a slit was visible. This created a recessed slit (∼5 μm from the surface). A slit 200 nm wide was fabricated using this method. Larger contact pad slits were cut at a lower magnification and higher ion current taking care not to damage the nanowire slit. After the nanostencil was fabricated, it was removed from the FIB and placed face down on a silicon nitride membrane. 5 nm of Ti and 30 nm of Au were evaporated at 5×10^{-6} Torr. The 200 nm nanostencil formed a 330 nm wide nanowire seamlessly connected to 5 μm wide contact pads (see figure 6). The nanowire is wider than the slit because the slit is recessed from the surface. FIB milling from the etch pit side would allow the nanostencil to be in closer contact with the surface reducing the increase in pattern size. We chose to etch from the front side to reduce the thickness of the silicon supporting the nanostencil to minimize potential clogging. No attempt was made to optimize the conditions for nanostencil deposition. Because of the unique design of the silicon supporting the nanostencil, the nanowire connected contact pads could be fabricated in a one step deposition process.

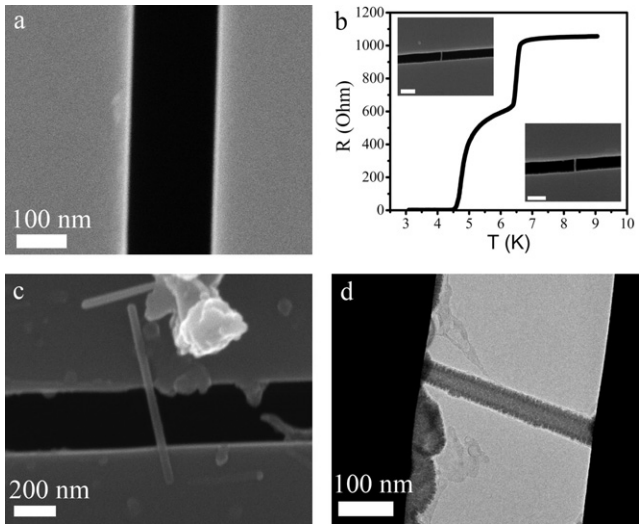

Figure 5. (a) SEM image of a TEM compatible 165 nm wide slit made by FIB milling from the etch pit side. The image is taken from the front side i.e. the side opposite the etch pit side. The SEM image was taken in a FEI Dual-Beam 235 FIB. (b) Resistance versus temperature measurement of two MoGe nanowires suspended on a TEM compatible slit made by FIB milling. The nanowires' superconducting transition is similar to wires prepared on conventional non-TEM compatible trenches indicating the stability of the slits. The insets show the two wires. The wires are formed by coating a single-walled carbon nanotube (SWNT) with MoGe. (c) A MoGe coated multi-walled nanotube (MWNT) spanning a FIB milled TEM compatible slit. (d) The same MoGe coated nanotube as in (c) imaged in 2010F JEOL TEM.

3. Discussion

Transparency photomasks are a relatively inexpensive and simple way to make microscale features. They typically

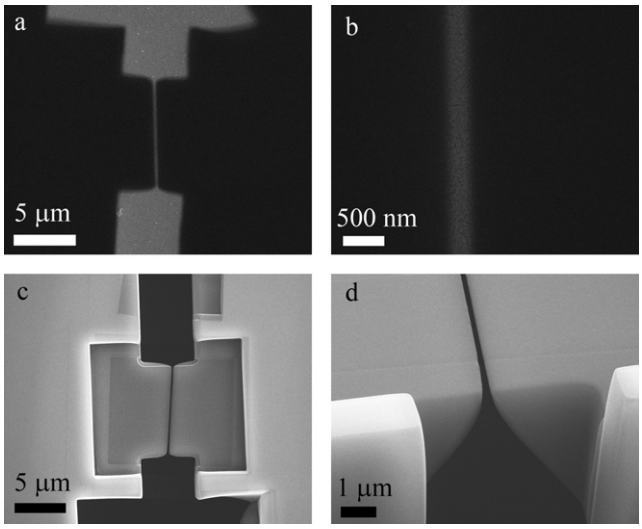

Figure 6. (a) 330 nm nanowire with seamless contact pads fabricated in one nanostencil deposition step. (b) Close-up of the 330 nm nanowire shown in (a). (c) The nanostencil used to make the nanowire shown in (a) and (b). The nanostencil was fabricated by FIB milling from the front side. The nanostencil consists of a narrow slit connected to two larger holes. When metal is evaporated through the nanostencil, a nanowire seamlessly connected to contact pads is formed. (d) Cross section of the nanostencil shown in (c). The sloped design makes this nanostencil more mechanically stable than one cut in a silicon nitride membrane.

have a minimum resolution of ∼5–10 μm. Using only transparency mask photolithography, sonication and wet etching, we have made ∼100 nm slits in silicon. We have demonstrated these slits can be used either for TEM samples compatible with electrical transport measurements or nanostencil lithography. This relates to other methods in which conventional microfabrication techniques are pushed into the nanoscale using unconventional approaches. For example, in phase-mask photolithography [20, 21], micron scale photolithography is extended down into the nanoscale by the destructive interference of light. In step edge lithography, micron scale photolithography is used to fabricate nanoscale wires [22, 23] along the edge of a smooth step by a combination of anisotropic deposition and anisotropic etching.

A variety of transmission electron microscope (TEM) compatible grids such as carbon, metal and silicon nitride membrane window grids exist. However, the majority of these samples are not compatible with both imaging in a TEM and performing electrical transport measurements, either simultaneously *in situ* or after imaging *ex situ*. At the same time, a strong interest in combining transport measurements with TEM imaging exists [24–27]. There is no obvious way to perform transport measurements on a sample deposited on a standard TEM carbon or metal grid. Silicon nitride membrane window grids can be adapted to allow transport measurements in at least two ways. First, slits can be formed (e.g. by focused ion beam milling) in the silicon nitride and the sample and electrodes can be deposited on the slit [28, 29]. The slit both suspends the sample for TEM imaging and separates the electrodes for transport measurements. However, making a slit through a thin membrane in this manner compromises the mechanical stability of the already flexible membrane. An alternate possibility is to make connections on top of the membrane (e.g. by electron beam lithography) and perform TEM imaging of the sample directly through the underlying membrane. This results in a significant loss in resolution of the TEM image due to the membrane present underneath the specimen. Although successful measurements have been made, the membranes themselves tend to be quite fragile and prone to breaking. The flexibility of the membrane can lead to poor contacts to the nano-object being measured, affecting the transport measurement.

A more rigid TEM substrate can be made by using a thicker membrane such as a silicon-on-insulator (SOI) membrane. In this thicker membrane, a slit can be etched, for example, by deep reactive ion etching (DRIE) [27, 30]. However, the large thickness of the silicon typically limits the slit width to ∼1 μm or more (assuming a 10:1 aspect ratio in a 10 μm thick membrane). Slits formed in SOI membranes by KOH etching are difficult to adapt for nanostencil lithography or TEM samples compatible with transport measurements because of the geometry of the samples [2–4]. While it may be possible to balance membrane thickness with small slit size, even a thicker membrane might still be too flexible to form high quality contacts to the nano-object being measured. An ideal TEM support compatible with transport measurements would be a long (10 μm or greater), narrow (∼100 nm) slit that quickly broadens out to a thicker support for improved mechanical stability. Our etched chips approximate this ideal. The sonication-induced slits allow us to easily measure and simultaneously TEM image a MWNT deposited on the slit. The FIB milled slits are stable enough to allow TEM imaging and subsequent cryogenic measurement of fragile superconducting nanowires.

Nanowires have been formed by nanostencil lithography before, primarily using slits in silicon nitride membranes [8–11]. However if one wishes to contact such a nanowire for electrical transport measurements, further fabrication steps are required to form contacts. The most obvious way to form contacts is by drilling larger holes in the silicon nitride membrane contacting the narrow slit. On a silicon nitride membrane, the flexibility of the membrane would affect the fidelity of the deposited nanostructure. Methods to improve the fidelity of silicon nitride membranes when tackling complex geometries have been described, by placing corrugated supports on the silicon nitride membranes [31]. Our slits are supported by a silicon chip so a nanostencil nanowire with seamless contacts can be deposited in a one step process.

4. Conclusion

We have fabricated macroscopic silicon chips penetrated by 100 nm scale slits. We have demonstrated two methods for making these slits, one using only microscale processing equipment and the other using FIB milling. We have demonstrated these slits have a variety of applications such as fabricating TEM compatible samples that are also compatible with electrical transport measurements and nanostencil deposition of nanowires seamlessly connected to contact pads.

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